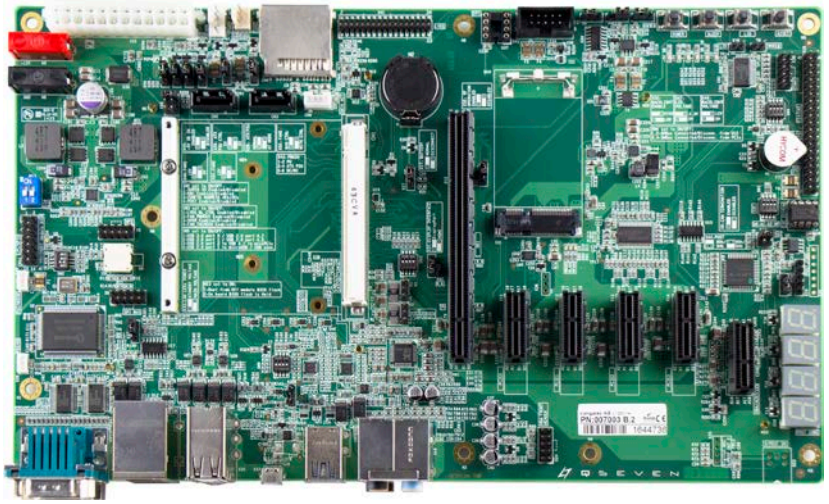

conga-QEVAL /Qseven® 2.0

Detailed description of the congatec Qseven® 2.0 evaluation carrier board

User's Guide

Revision 1.1

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
1.0	2014.05.09	AEM	• Official release
1.1	2015.01.15		• Updated section 5.2.7 “Universal Serial Bus (USB)”. • Updated the User’s Guide to revision B.2.

Preface

This user's guide provides information about the components, features and connectors available on the conga-QEVAL/Qseven® 2.0 evaluation carrier board.

The conga-QEVAL/Qseven® 2.0 module is referred to as QEVAL 2.0 throughout this document.

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Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Connector Type

Describes the connector that must be used with the Qseven® 2.0 evaluation carrier board, not the connector found on the Qseven® evaluation carrier board.

Link to connector layout diagram

This link icon is located in the top left corner of each page. It provides a direct link to the connector layout diagram on page 10 of this document.

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Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 or x16 link.
PCI Express Mini Card	PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms.
MMCplus	MMCplus was defined for first time in MMC System Specification v4.0. MMCplus is backward compatible with MMC. MMCplus has 13 pins.
SDIO card	SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
S/PDIF	S/PDIF (Sony/Philips Digital Interconnect Format) specifies a Data Link Layer protocol and choice of Physical Layer specifications for carrying digital audio signals between devices and stereo components.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
LPC	Low Pin-Count: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus: is a popular derivative of the I²C-bus.
CAN	Controller Area Network
SPI	Serial Peripheral Interface
GBE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

Contents

1 Introduction

1.1 Qseven® 2.0 Concept

The Qseven® concept is an off-the-shelf, multi vendor, Computer-on-Module that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have standardized form factors of 70mm x 70mm and 70mm x 40mm, and specified pinout based on the high speed MXM system connector. The pinout is the same for all vendors. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

1.2 QEVAL 2.0

QEVAL 2.0 evaluation carrier board is designed according to Qseven® specification 2.0 and supports both x86 and ARM modules. With this dual architecture support, customers can test modules with different architectures on a single carrier board, thereby reducing production cost and time.

The customers however need to make sure the switches and jumpers for the shared pins are set correctly to avoid possible malfunction or damage to the module/carrier board.

2 Jumper and DIP Switch Settings

Default Jumper and DIP Switch Settings for QEVAL 2.0

Jumper	Default
X9	2-3
X17	1-2
X22	1-2
X28	1-2
X29	1-2
X32	1-2
X33	1-2
X37	1-2
X43	1-2

Jumper	Default
X44	1-2
X46	1-2
X47	2-3
X48	1-2
X49	1-2
X50	1-2
X51	1-2
X52	1-2

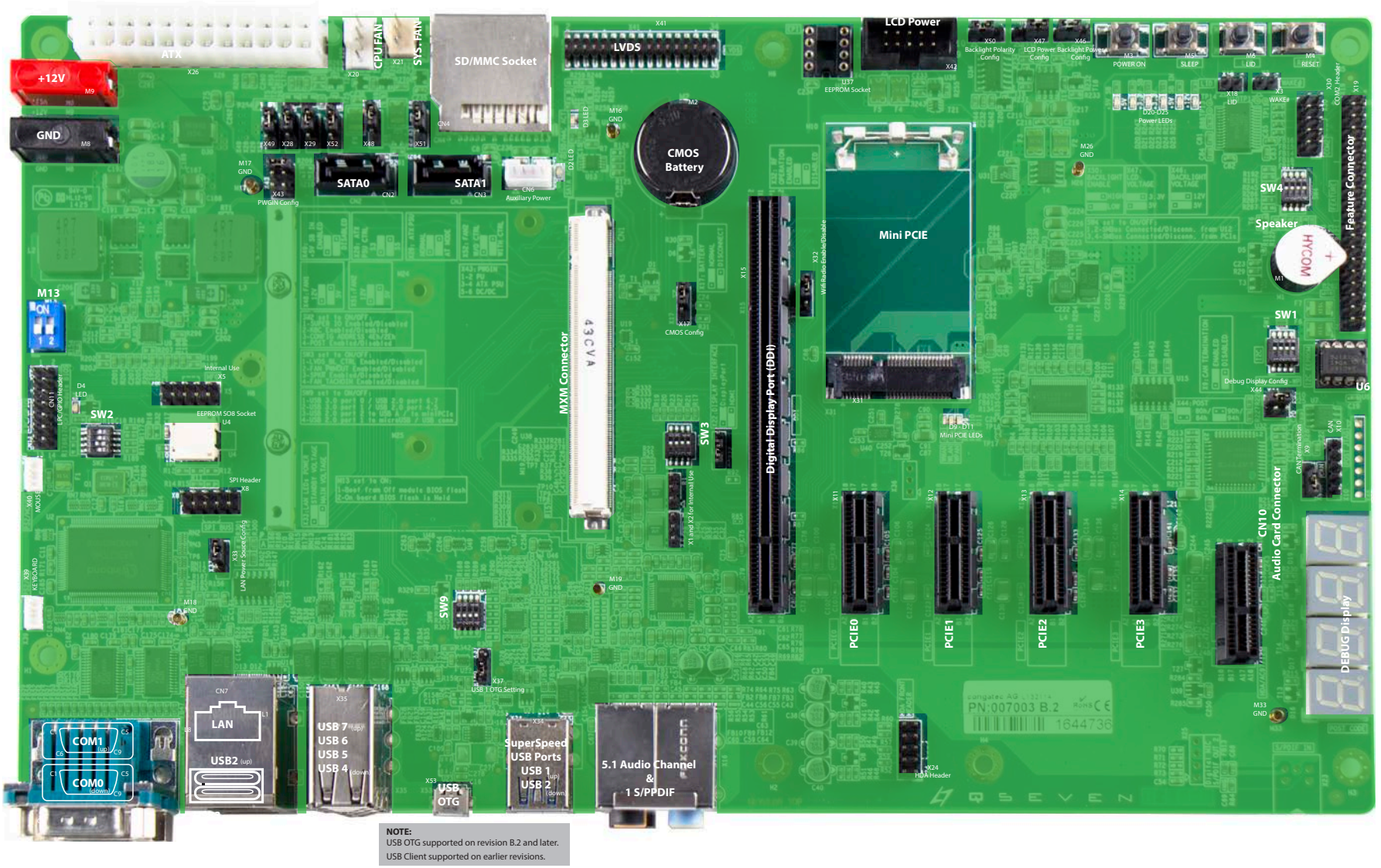
DIP Switch	Switch 1	Switch 2	Switch 3	Switch 4
SW1	ON	ON	ON	ON
SW2	ON	ON	OFF	ON
SW3	ON	ON	ON	ON
SW4	ON	ON	ON	ON
SW9	OFF	OFF	OFF	OFF
M13	OFF	OFF		

Required DIP Switch Settings when using conga-QMX6

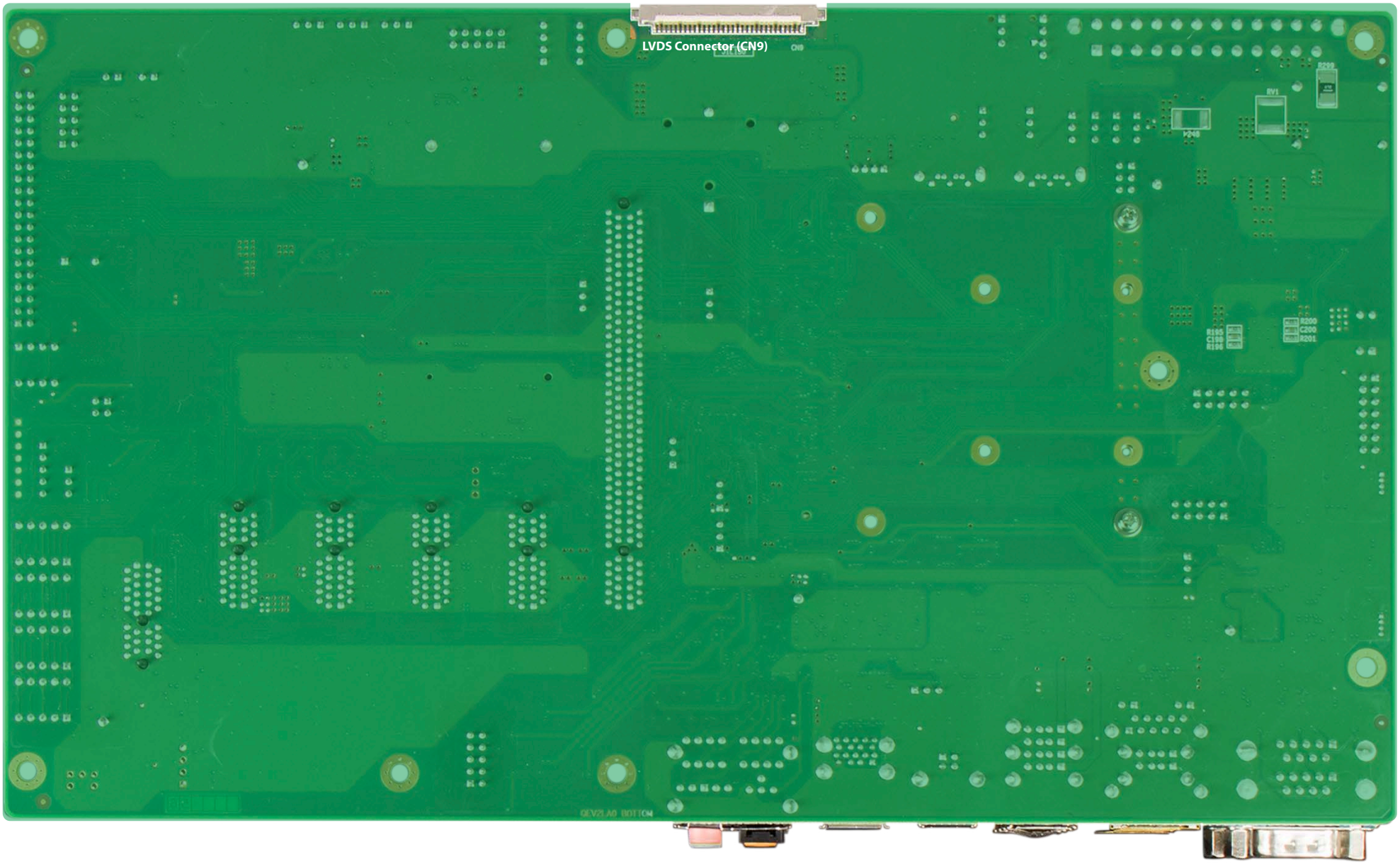
DIP Switch	Switch 1	Switch 2	Switch 3	Switch 4	Comment
SW1	OFF	OFF	OFF	OFF	
SW2	OFF	OFF	OFF	OFF	conga-QMX6 does not support LPC Bus.
SW3	ON	OFF	OFF	OFF	FAN_PWMOUT / SPKR / FAN_TACHOIN signals are routed to a GPIO of the i.MX6 SoC (the signals must be implemented in the Kernel first before they can be functional)
SW4	ON	ON	ON	ON	
SW9	OFF	OFF	OFF	OFF	
M13	OFF (BOOT_ALT# Jumper)	OFF			Dip 1 of Switch M13 must be set to ‘ON’ when updating the conga-QMX6 bootloader.

3 Connector Layout

The connector layout picture below shows each connector and its name designator. The Jumpers are also shown. Select the Adobe 'Zoom-In-Tool' and zoom in on a given component to see its designator. Hover over the component and the 'Zoom-In-Tool' will change indicating there is a link. Click on the link to navigate to the area in the document where the component is described. Use the mouse icon in the top left hand corner of the destination page to return to the connector layout picture.



Connector Layout Bottom Side



4 Specifications

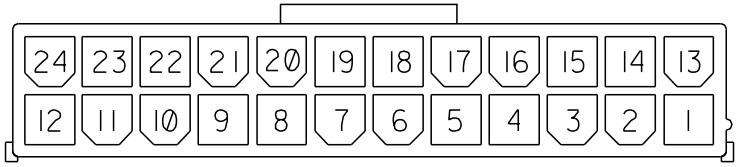
4.1 Mechanical Dimensions

- 293.4mm x 171.5mm
- Height approximately 37mm

4.2 Power Supply

The QEVAL 2.0 can be used with standard ATX (Connector X26) power supplies. The 3.3V, 5V and -12V power outputs of the ATX power supply are not used.

ATX Power Connector (X26)



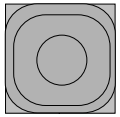
Connector X26 Pinout Description

Pin	Signal	Description	Pin	Signal	Description
1	+3.3V	Power Supply +3.3VDC	13	+3.3V	Power Supply +3.3VDC
2	+3.3V	Power Supply +3.3VDC	14	-12V	Power Supply -12VDC
3	GND	Power Ground	15	GND	Power Ground
4	+5V	Power Supply +5VDC	16	PS_ON#	Power Supply On (active low). Short this pin to GND to switch power supply ON, disconnect from GND to switch OFF.
5	GND	Power Ground	17	GND	Power Ground
6	+5V	Power Supply +5VDC	18	GND	Power Ground
7	GND	Power Ground	19	GND	Power Ground
8	PWR_OK	Power Ok: A status signal generated by the power supply to notify the computer that the DC operating voltages are within the ranges required for proper computer operation.	20	NC	Not connected
9	5V_SB	Standby Power Supply +5VDC	21	+5V	Power Supply +5VDC
10	+12V	Power Supply +12DC	22	+5V	Power Supply +5VDC
11	+12V	Power Supply +12DC	23	+5V	Power Supply +5VDC
12	+3.3V	Power Supply +3.3VDC	24	GND	Power Ground

When using an ATX power supply, the Qseven® module starts after you press the power-on button M3. The ATX power supply can also be used in AT mode. In this case the module starts when you turn on the power supply. Configure the power supply to ATX or AT mode with Jumper X29.

Jumper X29	Configuration
1 - 2	ATX Power supply (default)
2 - 3	ATX Power supply runs in AT mode

Pwr On (M3)



Power Mode Config (X29)

Connector Type

X29 : 2.54mm grid Jumper.

You can isolate the carrier board's 5V standby power supply from the ATX 5V standby power supply with the Jumper X49. The isolation is ideal for test purposes.

Jumper X49	Configuration
1 - 2	+5V_SB from ATX PSU enabled (default)
2 - 3	+5V_SB from ATX PSU disabled

Jumper X49

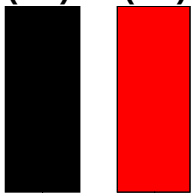
Connector Type

X49 : 2.54mm grid Jumper.

The QEVAL 2.0 can also be used with +12VDC power supply (connector M8 and M9). The +3.3V and +5V used by some devices on the QEVAL 2.0 are generated onboard from the +12V power supply.

Connector	Configuration
M8	Ground
M9	+12VDC ±5%

GND (M8) **+12V (M9)**



Connector Type

M8,M9: 4mm diameter plug

4.2.1 PWR_OK Signal

The PWR_OK (PWGIN) signal is a HIGH active input from the main power supply to the module and indicates whether the power is good. The Jumper X43 on the QEVAL 2.0 provides the ability to choose different settings for this signal.

Jumper X43	Configuration
1 - 2	PWGIN generated by Pull-up resistor. (default)
3 - 4	PWGIN generated by ATX power source.
5 - 6	PWGIN generated by DC/DC converter.

PWGIN Config. (X43)

Connector Type

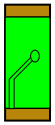
X43: 2.54mm grid Jumper.

4.2.2 Power Status LEDs D20-D25

The six green status LEDs D20-D25 indicate different power states of the QEVAL 2.0. See table below for more information.

LEDs D20-D25	Power state
All Off	No power applied.
D20	+5V standby
D21	+5V
D22	+3.3V standby
D23	+3.3V
D24	+5V standby input
D25	+12V input

D20-D25



4.2.3 Power-up Control

The native system Power-up support of Qseven® modules uses the *'SUS_S3#'* signal to control the *'PS_ON#'* signal, which is used to switch the ATX power supply on or off. When using the *SUS_S3#'* signal, the Qseven® module is capable of supporting Suspend to RAM (S3).

When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through the use of an inverter, the low active *'PS_ON#'* signal goes high and switches off the ATX power supply. On the contrary, if the system resides in a power-down system state, any system wake-up event invokes the chipset of the module to deassert the *'SUS_S3#'* signal. This transitions the system to Full-On (S0).

The way Suspend to RAM is implemented on a Qseven® module may differ depending on the module manufacturer. For this reason, it is

recommended to implement a hardware Jumper on the carrier board, to provide the ability to choose if the *'PS_ON#'* signal should be controlled by the *'SUS_S3#'* signal or the '*SUS_S5#'* signal. On the QEVAL 2.0, this is accomplished through the use of Jumper X28.

Jumper X28	Configuration
1 - 2	ATX Power supply controlled via S3# (default)
2 - 3	ATX Power supply controlled via S5#

Control signal Config (X28)

Connector Type

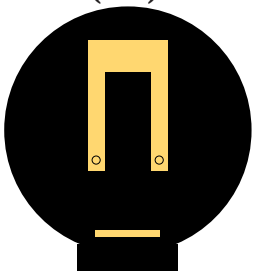
X28 : 2.54mm grid Jumper.

4.3 CMOS Battery

The CMOS battery on connector M2 supplies power to the RTC and CMOS memory of the Qseven® module. The battery needs to provide 3V of power. The specified battery type is CR2032. It is possible to disconnect the CMOS battery using Jumper X17.

Jumper X17	Configuration
1 - 2	Normal operation, battery connected (default)
2 - 3	Battery disconnected

CMOS Battery (M2)



CMOS Battery Config (X17)

Connector Type

X17 : 2.54mm grid Jumper.

Warning

Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Note

To fulfill the requirements of the EN60950, the QEVAL 2.0 incorporates two current-limiting devices (resistor and diode) in the battery power supply path.

4.4 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Note

The above operating temperatures must be strictly adhered to at all times.

Humidity specifications are for non-condensing conditions.

5 Connector Description

5.1 Connector CN1 Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5	SDIO Data Line 5
53	SDIO_DAT4	SDIO Data Line 4	54	SDIO_DAT7	SDIO Data Line 7
55	SDIO_DAT6	SDIO Data Line 6	56	RSVD	Reserved
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC / AC97_SYNC / I2S_WS	Serial Bus Synchronization. Serial Bus Synchronization Multiplexed with I2S Word Select	60	SMB_CLK / GP1_I2C_CLK	SMBus Clock line. Multiplexed with General Purpose I²C bus #1 clock line

Pin	Signal	Description	Pin	Signal	Description
61	HDA_RST# / AC97_RST# / I2S_RST#	HD Audio Codec Rest AC'97 Codec Reset. Multiplexed with I2S Codec Reset	62	SMB_DAT / GP1_I2C_DAT	SMBus Data line. Multiplexed with General Purpose I²C bus #1 data line.
63	HDA_BCLK / AC97_BCLK / I2S_CLK	HD Audio Serial Bit Clock AC'97 Serial Bit Clock. Multiplexed with I2S Serial Data Clock	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI / AC97_SDI / I2S_SDI	HD Audio Serial Data Input AC'97 Serial Data Input. Multiplexed with I2S Serial Data Input	66	GP0_I2C_CLK	General Purpose I2C Bus No 0 clock line
67	HDA_SDO / AC97_SDO / I2S_SDO	HD Audio Serial Data Output AC'97 Serial Data Output. Multiplexed with I2S Serial Data Output.	68	GP0_I2C_DAT	General Purpose I2C Bus No 0 data line
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7- / USB_SSTX0-	USB Port 7 Differential Pair- . Multiplexed with Superspeed USB transmit differential pair-	76	USB_P6- / USB_SSRX0-	USB Port 6 Differential Pair-. Multiplexed with Superspeed USB receive differential pair-
77	USB_P7+ / USB_SSTX0+	USB Port 7 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	78	USB_P6+ / USB_SSRX0+	USB Port 6 Differential Pair+. Multiplexed with Superspeed USB receive differential pair+
79	USB_6_7_OC#	Over current detect input for USB port 6 and 7	80	USB_4_5_OC#	Over current detect input for USB port 4 and 5
81	USB_P5- / USB_SSTX1-	USB Port 5 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-	82	USB_P4- / USB_SSRX1-	USB Port 4 Differential Pair-. Multiplexed with Superspeed USB receive differential pair-
83	USB_P5+ / USB_SSTX1+	USB Port 5 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	84	USB_P4+ / USB_SSRX1+	USB Port 4 Differential Pair+. Multiplexed with Superspeed USB receive differential pair+
85	USB_2_3_OC#	Over current detect input for USB port 2 and 3	86	USB_0_1_OC#	Over current detect input for USB port 0 and 1
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_CC	USB Client present detect pin	92	USB_ID	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	eDP0_TX0+ / LVDS_A0+	eDP Primary Channel 0+ LVDS Primary channel 0+	100	eDP1_TX0+ / LVDS_B0+	eDP Secondary channel 0+ LVDS Secondary channel 0+
101	eDP0_TX0- / LVDS_A0-	eDP Primary channel 0- LVDS Primary channel 0-	102	eDP1_TX0- / LVDS_B0-	eDP Secondary channel 0- LVDS Secondary channel 0-
103	eDP0_TX1+ / LVDS_A1+	eDP Primary channel 1+ LVDS Primary channel 1+	104	eDP1_TX1+ / LVDS_B1+	eDP Secondary channel 1+ LVDS Secondary channel 1+
105	eDP0_TX1- / LVDS_A1-	eDP Primary channel 1- LVDS Primary channel 1-	106	eDP1_TX1- / LVDS_B1-	eDP Secondary channel 1- LVDS Secondary channel 1-
107	eDP0_TX2+ / LVDS_A2+	eDP Primary channel 2+ LVDS Primary channel 2+	108	eDP1_TX2+ / LVDS_B2+	eDP Secondary channel 2+ LVDS Secondary channel 2+

Pin	Signal	Description	Pin	Signal	Description
109	eDP0_TX2- / LVDS_A2-	eDP Primary channel 2- LVDS Primary channel 2-	110	eDP1_TX2- / LVDS_B2-	eDP Secondary channel 2- LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	eDP0_TX3+ / LVDS_A3+	eDP Primary channel 3+ LVDS Primary channel 3+	114	eDP1_TX3+ / LVDS_B3+	eDP Secondary channel 3+ LVDS Secondary channel 3+
115	eDP0_TX3- / LVDS_A3-	eDP Primary channel 3- LVDS Primary channel 3-	116	eDP1_TX3- / LVDS_B3-	eDP Secondary channel 3- LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	eDP0_AUX+ / LVDS_A_CLK+	eDP Primary Auxilliary channel+ LVDS Primary channel CLK+	120	eDP1_AUX+ / LVDS_B_CLK+	eDP Secondary Auxiliary channel CLK+ LVDS Secondary channel CLK+
121	eDP0_AUX- / LVDS_A_CLK-	eDP Primary Auxilliary channel- LVDS Primary channel CLK-	122	eDP1_AUX- / LVDS_B_CLK-	eDP Secondary Auxiliary channel CLK- LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	GP_1-Wire_Bus	General Purpose 1-wire bus interface
125	LVDS_DID_DAT / GP2_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	eDP0_HPD# / LVDS_BLC_DAT	SSC clock chip data line. Can be used as eDP primary hotplug detect
127	LVDS_DID_CLK / GP2_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	eDP1_HPD# / LVDS_BLC_CLK	SSC clock chip clock line. Can be used as eDP secondary hotplug detect
129	CAN0_TX	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX	CAN RX Input for CAN Bus Channel 0
131	DP_LANE3+ / TMDS_CLK+	DisplayPort differential pair line lane 3+. Multiplexed with TMDS differential pair clock+	132	RSVD (Differential)	Reserved
133	DP_LANE3- / TMDS_CLK-	DisplayPort differential pair line lane 3-. Multiplexed with TMDS differential pair clock-	134	RSVD (Differential)	Reserved
135	GND	Power Ground	136	GND	Power Ground
137	DP_LANE1+ / TMDS_LANE1+	DisplayPort differential pair line lane 1+ Multiplexed with TMDS differential pair lane1+	138	DP_AUX+	DisplayPort auxiliary channel
139	DP_LANE1- / TMDS_LANE1-	DisplayPort differential pair line lane 1- Multiplexed with TMDS differential pair lane1-	140	DP_AUX-	DisplayPort auxiliary channel
141	GND	Power Ground	142	GND	Power Ground
143	DP_LANE2+ / TMDS_LANE0+	DisplayPort differential pair line lane 2+ Multiplexed with TMDS differential pair line lane0+	144	RSVD (Differential Pair)	Reserved
145	DP_LANE2- / TMDS_LANE0-	DisplayPort differential pair line lane 2- Multiplexed with TMDS differential pair line lane0-	146	RSVD (Differential Pair)	Reserved
147	GND	Power Ground	148	GND	Power Ground
149	DP_LANE0+ / TMDS_LANE2+	DisplayPort differential pair line lane 0+ Multiplexed with TMDS differential pair lane2+	150	HDMI_CTRL_DAT	DDC based control signal (data) for HDMI/DVI device.
151	DP_LANE0- / TMDS_LANE2-	DisplayPort differential pair line lane 0- Multiplexed with TMDS differential pair lane2-	152	HDMI_CTRL_CLK	DDC based control signal (clock) for HDMI/DVI device.
153	DP_HDMI_HPD#	Hot plug detection	154	DP_HPD	DisplayPort Hot Plut Detect
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground

Pin	Signal	Description	Pin	Signal	Description
161	PCIE3_TX+	PCI Express Channel 3 Output+	162	PCIE3_RX+	PCI Express Channel 3 Input+
163	PCIE3_TX-	PCI Express Channel 3 Output-	164	PCIE3_RX-	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	UART0_TX	Serial Data Transmitter	172	UART0_RTS#	Request To Send handshake signal
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	UART0_RX	Serial Data Receiver	178	UART0_CTS#	Clear To Send handshake signal
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0 / GPIO0	LPC Interface Address Data 0 General Purpose input/output 0	186	LPC_AD1 / GPIO1	LPC Interface Address Data 1 General Purpose input/output 1
187	LPC_AD2 / GPIO2	LPC Interface Address Data 2 General Purpose input/output 2	188	LPC_AD3 / GPIO3	LPC Interface Address Data 3 General Purpose input/output 3
189	LPC_CLK /GPIO4	LPC Interface Clock General Purpose input/output 4	190	LPC_FRAME# /GPIO5	LPC frame indicator General Purpose input/output 5
191	SERIRQ /GPIO6	Serialized interrupt General Purpose input/output 6	192	LPC_LDRQ# /GPIO7	LPC DMA request General Purpose input/output 7
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN /GP_TIMER_IN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI	SPI Master serial output/Slave serial input	200	SPI_CS0#	SPI Chip Select 0 Output
201	SPI_MISO	SPI Master serial input/Slave serial output signal	202	SPI_CS1#	SPI Chip Select 1 Output
203	SPI_SCK	SPI Clock Output	204	MFG_NC4	For manufacturing and debugging purposes
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	For manufacturing and debugging purposes	208	MFG_NC2	For manufacturing and debugging purposes
209	MFG_NC1	For manufacturing and debugging purposes	210	MFG_NC3	For manufacturing and debugging purposes
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

5.2 Subsystems of QEVAL 2.0

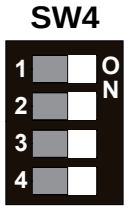
5.2.1 SMBus

The QEVAL 2.0 supports both SMBus and I2C compliant devices. The SMBus signals are available in different locations on the QEVAL 2.0, including the feature connector (X19) described in section 6.13 of this document.

Use DIP switch SW4 on the QEVAL 2.0 to connect or disconnect SMBus devices that are not compatible with the I2C bus. For example, when you insert a Qseven® module that supports I2C bus on the QEVAL 2.0 instead of the SMBus (e.g conga-QMX6), then set SW4 DIP switches to OFF. This setting disconnects the SMBus devices.

DIP Switch SW4 Pin Description

DIP Switch	Status	Description
1	ON OFF	Connect module's SMB clock signal to PCIe clock buffer Disconnect module's SMB clock signal from PCIe clock buffer
2	ON OFF	Connect module's SMB data signal to PCIe clock buffer Disconnect module's SMB data signal from PCIe clock buffer
3	ON OFF	Connect module's SMB clock signal to PCIe Slots Disconnect module's SMB clock signal from PCIe Slots
4	ON OFF	Connect module's SMB data signal to PCIe clock buffer Disconnect module's SMB data signal from PCIe clock buffer



Default Settings:
ALL ON

5.2.2 I²C Bus

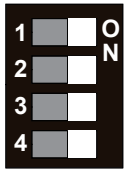
The I²C signals are available in different locations on the QEVAL 2.0 including the feature connector (X19) described in section 6.13 of this document. Additionally, the QEVAL 2.0 includes a socket for an I²C EEPROM (U6) that can be used for test purposes during the system development.

The 8 pin DIP socket can be used with various 2-wire serial EEPROMS such as 24C04/08/16 and can be easily accessed by using the I²C control commands implemented in the Qseven® EASI API driver. Refer to the Qseven® module's user's guide and the EASI programmers guide for more information.

The address inputs (A0-A2) and write protect (WP) pin of I²C EEPROM can be configured with DIP switch SW1. By default, the DIP switches are set to ON (LOW state).

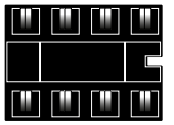
DIP Switch	Status	Description
1	ON OFF	Address input A0 set to LOW Address input A0 set to HIGH
2	ON/ OFF	Address input A1 set to LOW Address input A1 set to HIGH
3	ON/ OFF	Address input A2 set to LOW Address input A2 set to HIGH
4	ON/ OFF	Write protect set to LOW Write protect set to HIGH

SW1



Default Settings:
ALL ON

U6
EEPROM Socket



5.2.3 SPI Bus

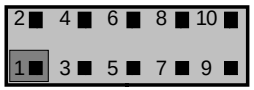
The QEVAL 2.0 provides connection to the Serial Peripheral Interface (SPI) Bus via connector X8 and SO8 socket. The 8 pin SO8 socket (connector U4) can be used for SPI EEPROM. For example, you can a 3.3V serial flash in the SO8 socket to boot the system from external BIOS. The write protect (WP#) and hold (HOLD#) pins of the SO8 socket are internally pulled up to allow normal read/write operations.

Use DIP switch M13 to select whether to boot from the QEVAL 2.0 onboard SPI flash or from the on-module SPI flash. The yellow LED D4 glows when module boots from SPI flash onboard the QEVAL 2.0 (off-module SPI flash). The chip select (CS#) signal on the SPI EEPROM socket is connected to the Qseven® module's SPI_CS0# signal and is active only if switch 1 of DIP switch M13 is turned on.

SPI connector X8

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	SPI_MOSI	4	SPI_CS0#
5	SPI_MISO	6	SPI_CS1#
7	SPI_SCK	8	N.C.
9	GND	10	GND

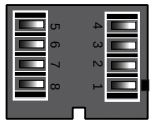
SPI Header (X8)



SO8 Socket U4

Pin	Signal	Pin	Signal
1	Chip Select Input	5	Data Input
2	Data Output	6	Serial Clock Input
3	Write Protect Input	7	Hold Input
4	GND	8	VCC

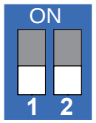
U4
EEPROM SO8 Socket



DIP Switch M13

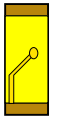
DIP Switch	Status	Description
1	ON OFF	Boot from SPI flash onboard the QEVAL 2.0 (off-module SPI flash) Boot from SPI flash onboard the Qseven® module (on-module SPI flash)
2	ON OFF	SPI flash (U4) on hold SPI flash (U4) in normal operation

M13



Default Settings:
ALL OFF

D4 LED



Connector Type

X8: 10 pin, 2 row 2.54mm grid female.

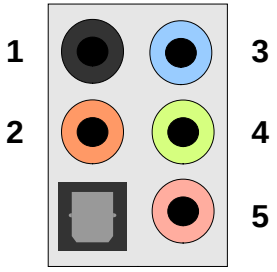
5.2.4 HDA Audio

The QEVAL 2.0 has a HDA (High Definition Audio) codec (Realtek ALC888S) mounted on it. The 5.1 channel audio output interface of this codec is available on the connector described below. The drivers for this codec can be found in the ‘Drivers’ section under ‘conga-QEVAL’ on the congatec website at www.congatec.com.

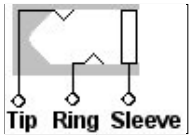
Audio X16

Stereo Jack 1	Signal	Stereo Jack 4	Signal
Tip	Surround Left	Tip	Line Output Left
Ring	Surround Right	Ring	Line Output Right
Sleeve	Analog Ground	Sleeve	Analog Ground
Stereo Jack 2	**Signal**	**Stereo Jack 5**	**Signal**
Tip	Center	Tip	Microphone Input Left
Ring	LFE	Ring	Microphone Input Right
Sleeve	Analog Ground	Sleeve	Analog Ground
Stereo Jack 3	**Signal**		
Tip	Line Input Left		
Ring	Line Input Right		
Sleeve	Analog Ground		

Audio (X16)



(front view)



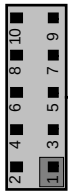
Connector Type

X16: 5 dedicated 3.5mm audio jacks (5.1 channel) and 1 optical S/PDIF output.

HDA Front Header Connector X24

Pin	Signal	Pin	Signal
1	Microphone 2 Input Left	2	Analog Ground
3	Microphone 2 Input Right	4	HDA_PRESENCE#
5	Line 2 Output Right	6	Microphone 2 Sense
7	Analog Ground	8	N.C.
9	Line 2 Output Left	10	Line 2 Sense

HDA Front Header (X24)



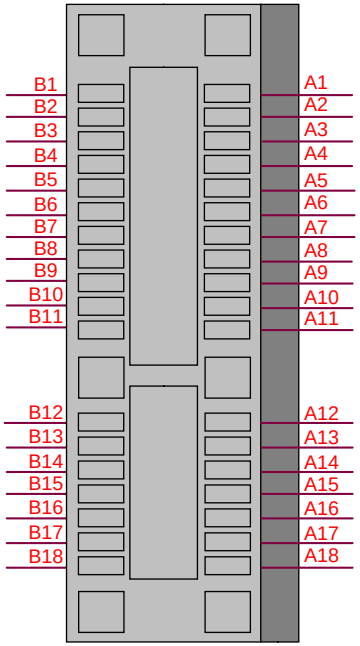
Connector Type

X24 10 pin, 2 row 2.54mm grid female.

The QEVAL 2.0 also provides an audio interface on an edge card connector (CN10) for additional HDA, AC'97 or I2S codec support.

Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT1#
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	I2C_CLK	A5	HDA_BCLK
B6	I2C_DAT	A6	HDA_SDOUT
B7	GND	A7	HDA_SDIN
B8	+3.3V	A8	HDA_SYNC
B9	HDA_RST#	A9	+3.3V
B10	+3.3V AUX	A10	+3.3V
B11	N.C.	A11	N.C.
	Key		
B12	SPKR	A12	GND
B13	GND	A13	N.C.
B14	N.C.	A14	N.C.
B15	N.C.	A15	GND
B16	GND	A16	N.C.
B17	PRSNT2#	A17	N.C.
B18	GND	A18	GND

HDA Edge Card Connector (CN10)



Note

The I2C signals at pins B5 and B6 are necessary for I2S audio codec support. The QEVAL 2.0 supports also optional S/PDIF digital input (X23) and S/PDIF output 2 (X25) interfaces. The connectors for these interfaces are not assembled by default.

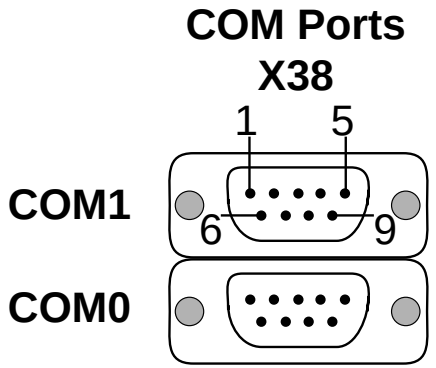
5.2.5 LPC Super I/O Device

The QEVAL 2.0 has an onboard Super I/O controller that provides additional interfaces such as two serial interfaces and KBC interface (mouse, keyboard). The Winbond W83627DHG Super I/O controller is connected to the LPC Bus of the Qseven® module.

5.2.5.1 COM Ports

The Super I/O controller provides two serial ports (COM0 and COM1) via connector X38. The serial ports are compliant to the RS232 standard and are only supported on modules that support LPC bus. For modules without LPC support, you can use the additional serial port (COM2), which is routed to header X30 for console functions. For more information about COM2 header, see section 6.8

Pin	COM0	COM1
1	DCD#	DCD#
2	RXD	RXD
3	TXD	TXD
4	DTR#	DTR#
5	GND	GND
6	DSR	DSR
7	RTS#	RTS#
8	CTS#	CTS#
9	RI#	RI#



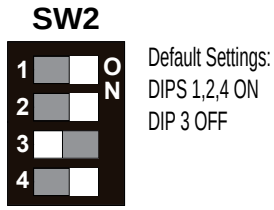
Connector Type

X38: 2x 9 pin D-SUB female.

With DIP switch SW2, you can disable the Super I/O or configure its base address. The following table describes the settings for SW2.

DIP Switch SW2

DIP Switch	Status	Configuration
1	ON/OFF	Super I/O Enabled/Disabled (ON=default)
2	ON/OFF	KBC Enabled/Disabled
3	ON/OFF	Super I/O configured for address 4Eh/2Eh
4	ON/OFF	Enable/disable POST display



Default Settings:
DIPS 1,2,4 ON
DIP 3 OFF

Note

Before you insert a module that does not support LPC (module with GPIO support such as conga-QMX6), you must set switch 1 and switch 4 of DIP switch SW2 to OFF. This setting turns off the onboard super I/O device.

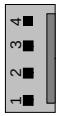
5.2.5.2 KBC Interface

The super I/O controller provides keyboard interface via connector X39 and mouse interface via connector X40. The PS2 mouse and keyboard are connected to the KBC interface of the Super I/O controller.

Keyboard (X39) Pin Description

Pin	Signal
1	Keyboard Clock
2	GND
3	+5V power supply
4	Keyboard Data

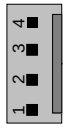
PS2 Kebooard (X39)



Mouse (X40) Pin Description

Pin	Signal
1	Mouse Clock
2	GND
3	+5V power supply
4	Mouse Data

PS2 Mouse (X40)



Connector Type

X39, X40: 4 pin 1.25mm pitch PicoBlade connectors (Molex).

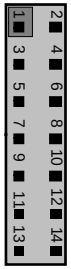
5.2.6 LPC/GPIO Header

To support LPC and GPIO devices, the LPC and GPIO signals are shared on the QEVAL 2.0. The shared signals are connected to pin header CN11. This header can be used for debugging or to connect devices such as Super I/O for evaluation.

LPC/GPIO Pin Description

Pin	LPC /GPIO	Pin	LPC /GPIO
1	LPC_AD0 / GPIO0	2	+5V supply
3	LPC_AD1 / GPIO1	4	+3.3V supply
5	LPC_AD2 / GPIO2	6	GND
7	LPC_AD3 / GPIO3	8	GND
9	LPC_CLK / GPIO4	10	LPC_LDRQ# / GPIO7
11	LPC_FRAME# / GPIO5	12	LPC_RST#
13	SERIRQ / GPIO6	14	BOOT_ALT#

LPC/GPIO Header CN11



Note

Before you insert a module that does not support LPC (module with GPIO support such as conga-QMX6), you must set switch 1 and switch 4 of DIP switch SW2 to "off". This setting turns off the onboard super I/O device.

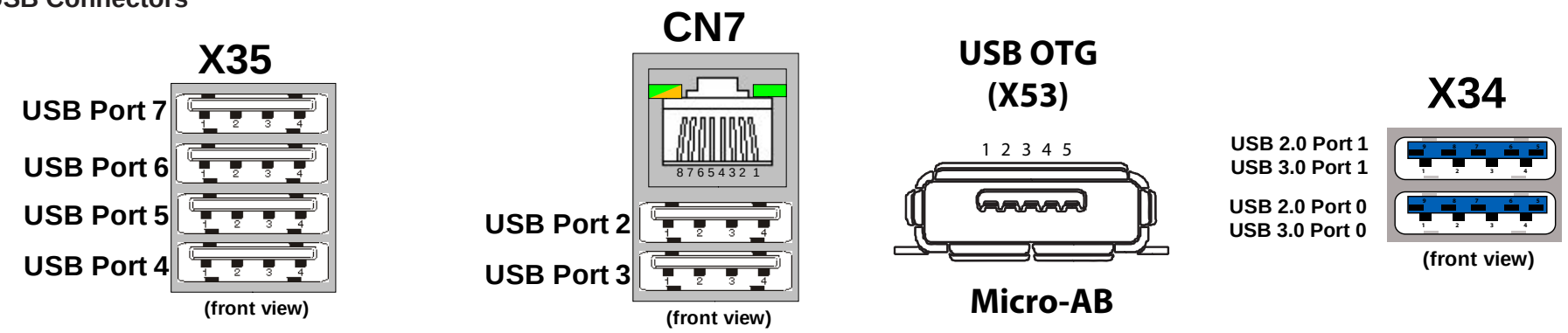
Connector Type

CN11: 14 pin, 2 row 2.54mm grid female.

5.2.7 Universal Serial Bus (USB)

The QEVAL 2.0 provides 8 USB host ports (connectors CN7, X35 and X34) and one USB OTG port (connector X53). The USB host ports 0 and 1 (X34) support USB 3.0 and are shared with USB 4-7 (X35) according to Qseven® 2.0 specification (Check the datasheet of the attached module to determine if USB3.0 or USB 2.0 is supported). The Superspeed signals of USB host port 0 are shared with ports 6 and 7 (X35) while the Superspeed signals of USB host port 1 are shared with port 4 and 5 (X35).

USB Connectors



Note

USB ports 2 and 3 support wake-on-USB. The support of USB port 3 wake-on-USB depends on the setting of DIP switch 9.3.

USB Pin Descriptions

USB 3.0 Pin Description (X34)			
Pin	Signal	Pin	Signal
1	+5V	5	USB3.0_SS_RX-
2	DATA-	6	USB3.0_SS_RX+
3	DATA+	7	USB3.0 GND
4	GND	8	USB3.0_SS_TX-
		9	USB3.0_SS_TX+

USB 2.0 Pin Description (X35, CN7)	
Pin	Signal
1	+5V
2	DATA-
3	DATA+
4	GND

USB OTG Pin Description (X53)	
Pin	Signal
1	VBUS
2	DATA-
3	DATA+
4	ID
5	GND

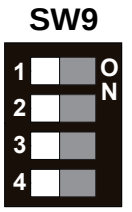
The possible USB configurations are:

- Up to 8x USB 2.0 (connectors CN7, X35 and X34 (only USB 2.0))
- Up to 5x USB 2.0 and 1x USB 3.0 (connectors CN7, ports 4,5 of X35 and port 0 of X34)
- Up to 2x USB 2.0 and 2x USB 3.0 (connectors CN7 and X34)
- Up to 7x USB 2.0 and 1x USB OTG
- Up to 4x USB 2.0, 1x USB 3.0 and 1x USB OTG

With DIP switch SW9, you can set the desired USB configuration as shown in the table below:

DIP Switch SW9

DIPs	Status	Description
1	ON OFF	Selects USB 3.0 port 0 (disables USB 2.0 port 6 and 7 of connector X35) Selects USB 2.0 port 6 and 7 (disables USB 3.0 port 0 of connector X34)
2	ON OFF	Selects USB 3.0 port 1 (disables USB 2.0 port 4 and 5 of connector X35) Selects USB 2.0 port 4 and 5 (disables USB 3.0 port 1 of connector X34)
3	ON OFF	Routes USB 2.0 signals to port 2 of connector CN7 (disables mini-PCIe) Routes USB 2.0 signals to mini-PCIe connector X31 (disables USB 2.0 port 2)
4	ON OFF	Routes USB 2.0 port 1 signals to connector X53 (micro USB AB connector) Routes USB 2.0 port 1 signals to standard USB A connector X34 (disables USB OTG support)



Default Settings:
ALL OFF

USB OTG Jumper Settings

Switch 4 of DIP switch 9 routes USB 2.0 port 1 signals to either connector X34 - a standard USB A connector or to connector X53 - a micro USB AB connector. For default USB host mode operation, set switch 4 of DIP switch 9 to OFF. This setting routes USB signals to connector X34 thereby disabling USB OTG support on connector X53. If a USB OTG capable module is attached (e.g conga-QMX6), you must additionally set Jumper X37 to position 2-3. This setting instructs the USB OTG capable module to operate in USB 'host only' mode.

For USB OTG operation, set switch 4 of DIP switch 9 to ON. Additionally, set Jumper X37 to position 1-2. This setting configures connector X53 for USB OTG mode operation. To configure connector X53 to 'host only' mode, set Jumper X37 to position 2-3. An auto detection mode will be implemented in newer revisions of QEVAL 2.0.

Jumper X37

Jumper X37	Configuration
1 - 2	sets USB port 1 (connector X53) to OTG mode
2 - 3	sets USB port 1 (connector X53) to host mode .

USB1 OTG Setting (X37)

Connector Type

X37: 2.54mm grid Jumper.

Note

The support of USB OTG on Qseven Computer-On-Module was introduced with Qseven Specification 2.0 Errata Sheet (Version E.2.0-001). To comply with the Errata Sheet, congatec implemented USB OTG in hardware revision B.2 of the QEVAL 2.0. Earlier revisions do not support USB OTG. For more information about the support of USB OTG, refer to QEVAL 2.0 hardware revision B.2 Errata Sheet (CTN 20141014 001. pdf) in the restricted area of the congatec website.

The USB configuration depends on the USB features supported on the attached module.

Caution

Modules that are Qseven® 2.0 compliant are not electrically compatible if their multi-function pins are configured differently. In addition, modules that are Qseven® specification 2.0 compliant may not be electrically backward compatible with modules that are Qseven® specification 1.x compliant. For this reason, if the Qseven® module being used supports USB 3.0, then you must ensure that DIP switch SW9 is configured properly. Failure to do this will cause damage to the Qseven® module and/or the QEVAL 2.0 evaluation carrier board.

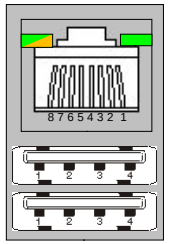
5.2.8 Ethernet 10/100/1000

The QEVAL 2.0 provides a LAN interface via connector CN7. The following tables describe the Ethernet pinout and jumper configuration.

RJ45 socket pinout

Pin	Signal	Pin	Signal
1	Bidirectional pair A+	2	Bidirectional pair A-
3	Bidirectional pair B+	4	Bidirectional pair C+
5	Bidirectional pair C-	6	Bidirectional pair B-
7	Bidirectional pair D+	8	Bidirectional pair D-

CN7



(front view)

RJ45 Socket LED descriptions

LED Left Side	Description
Off	10 Mbps link speed
Green	100 Mbps link speed
Orange	1000 Mbps link speed

LED Right Side	Description
Off	No link
Steady On	Link established, no activity detected
Blinking	Link established, activity detected

Jumper X33 determines the power source for the LAN LED drivers. Therefore, set this jumper according to the voltage source of the onboard module's LAN controller.

Jumper X33	Description
1 - 2	LAN controller is powered from standby voltage (default)
2 - 3	LAN controller is powered from main voltage

LAN Power Source Config (X33)

Connector Type

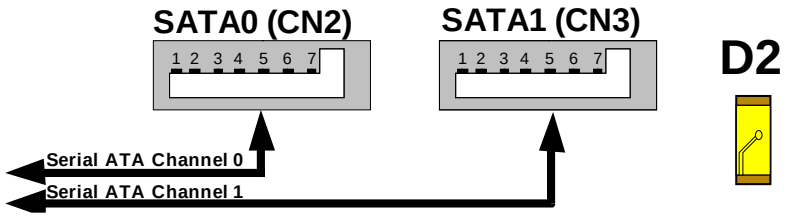
CN7: 8 pin RJ45 plug

X33: 2.54mm grid Jumper

5.2.9 Serial ATA™

The QEVAL 2.0 provides two SATA drive connectors, CN2 and CN3. The yellow LED D2 indicates when there is activity on either of the SATA interfaces. The following table describes the pinout of the SATA connectors.

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



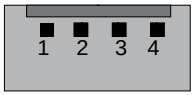
5.2.10 Serial ATA™ Auxiliary Power

The QEVAL 2.0 provides connector CN6 for 2.5” SATA auxiliary power. This connector supplies 3.3V and 5V only. You can order the auxiliary power cable with PN: 14000032 from congatec AG. For more information, contact congatec sales department.

CN6 Pinout Description

Pin	Signal
1	+3.3V
2	GND
3	GND
4	+5V

Auxiliary Power Connector (CN6)



Note

The connector CN6 does not support 3.5” SATA disks.

Connector Type

CN6: 4 pin 2mm pitch spacing PH connector (JST)

5.2.11 LVDS Flat Panel Interface

The QEVAL 2.0 provides two different connectors for LVDS - connectors X41 and CN9 (CN9 is located on the bottom side of the QEVAL 2.0).

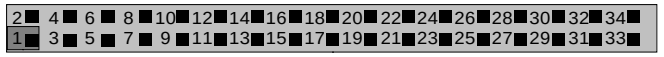
Connector X41 Signal Description

Pin	LVDS Output	Description	Pin	LVDS Output	Description
1	LVDS_DID_DAT	DisplayID DDC data line used for LVDS flat panel detection.	2	LVDS_DID_CLK	DisplayID DDC clock line used for LVDS flat panel detection.
3	N.C.		4	N.C.	
5	GND	Power Ground	6	LVDS_A0-	LVDS Channel A differential pairs
7	LVDS_A0+	LVDS Channel A differential pairs	8	LVDS_PPEN	Controls panel power enable
9	LVDS_A1-	LVDS Channel A differential pairs	10	LVDS_A1+	LVDS Channel A differential pairs
11	LVDS_BLEN	Controls backlight enable. (see Jumper CN14)	12	LVDS_A2+	LVDS Channel A differential pairs
13	LVDS_A2-	LVDS Channel A differential pairs	14	N.C.	
15	LVDS_A_CLK-	LVDS Channel A differential clock	16	LVDS_A_CLK+	LVDS Channel A differential clock
17	N.C.		18	LVDS_A3+	LVDS Channel A differential pairs
19	LVDS_A3-	LVDS Channel A differential pairs	20	GND	
21	LVDS_B0-	LVDS Channel B differential pairs	22	LVDS_B0+	LVDS Channel B differential pairs
23	GND	Power Ground	24	LVDS_B1-	LVDS Channel B differential pairs
25	LVDS_B1+	LVDS Channel B differential pairs	26	GND	Power Ground
27	LVDS_B2-	LVDS Channel B differential pairs	28	LVDS_B2+	LVDS Channel B differential pairs
29	GND	Power Ground	30	LVDS_B_CLK+	LVDS Channel B differential clock
31	LVDS_B_CLK-	LVDS Channel B differential clock	32	N.C.	
33	LVDS_B3+	LVDS Channel B differential pairs	34	LVDS_B3-	LVDS Channel B differential pairs

Connector Type

X41: 34 pin, 2 row 2mm grid female.

LVDS
(X41)



Connector CN9 Pin Description

Pin	LVDS Output	Pin	LVDS Output
1	GND	17	LVDS_B1+
2	LVDS_A0-	18	GND
3	LVDS_A0+	19	LVDS_B2-
4	LVDS_A1-	20	LVDS_B2+
5	LVDS_A1+	21	LVDS_B_CLK-
6	LVDS_A2-	22	LVDS_B_CLK+
7	LVDS_A2+	23	LVDS_B3-
8	GND	24	LVDS_B3+
9	LVDS_A_CLK-	25	GND
10	LVDS_A_CLK+	26	LVDS_DID_DAT
11	LVDS_A3-	27	LVDS_PPEN
12	LVDS_A3+	28	LVDS_DID_CLK
13	LVDS_B0-	29	VDD_LCD (750mA Fuse)
14	LVDS_B0+	30	VDD_LCD (750mA Fuse)
15	GND	31	VDD_LCD (750mA Fuse)
16	LVDS_B1-	32	GND

LVDS Connector (CN9)

Connector Type

CN9: JAE FI-X30SSL-HF, 32 pin, single row, 1mm pitch spacing (compatible with JILI30).

With Jumper X50, you can set up the polarity of the backlight enable signal 'LVDS_BLEN' from the Qseven® module.

Jumper X50	Configuration
1 - 2	Backlight enable HIGH active (default)
2 - 3	Backlight enable LOW active

Backlight Polarity Config (X50)

Connector Type

X50: 2.54mm grid Jumper.

5.2.11.1 Flat Panel and Backlight Power Supply

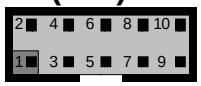
The power supply for flat panels and their backlight inverter is available on connector X42. Analog backlight control (BL_CTRL_AN) is also available via connector X42. To select panel and backlight voltage, use Jumpers X46 and X47. With switch 1 of DIP SW3, you can enable or disable the backlight control.

The tables below describes the pinout for connector X42, Jumpers X46 and X47. For the flat panel and backlight power supply connection, see the next page.

Connector X42 pinout

Pin	Signal	Pin	Signal
1	VDD_LCD (750mA Fuse)	2	VDD_BL (2A Fuse)
3	+5V (2A Fuse)	4	+12V (2A Fuse)
5	LVDS_PPEN	6	LVDS_BLEN
7	BL_CTRL_AN	8	BL_CTRL
9	GND	10	GND

LCD Power (X42)



Connector Type

X42: 10 pin, 2 row 2.54 mm grid female.

Jumper X46	Configuration
1 - 2	+12VDC Backlight Voltage (default)
2 - 3	+5VDC Backlight Voltage

Backlight Power Config (X46)

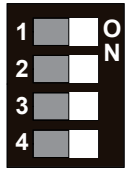
Jumper X47	Configuration
1 - 2	+3.3VDC LCD Voltage
2 - 3	+5VDC LCD Voltage (default)

LCD Power Config (X47)

Connector Type

X46 and X47 2.54mm grid Jumpers.

SW3

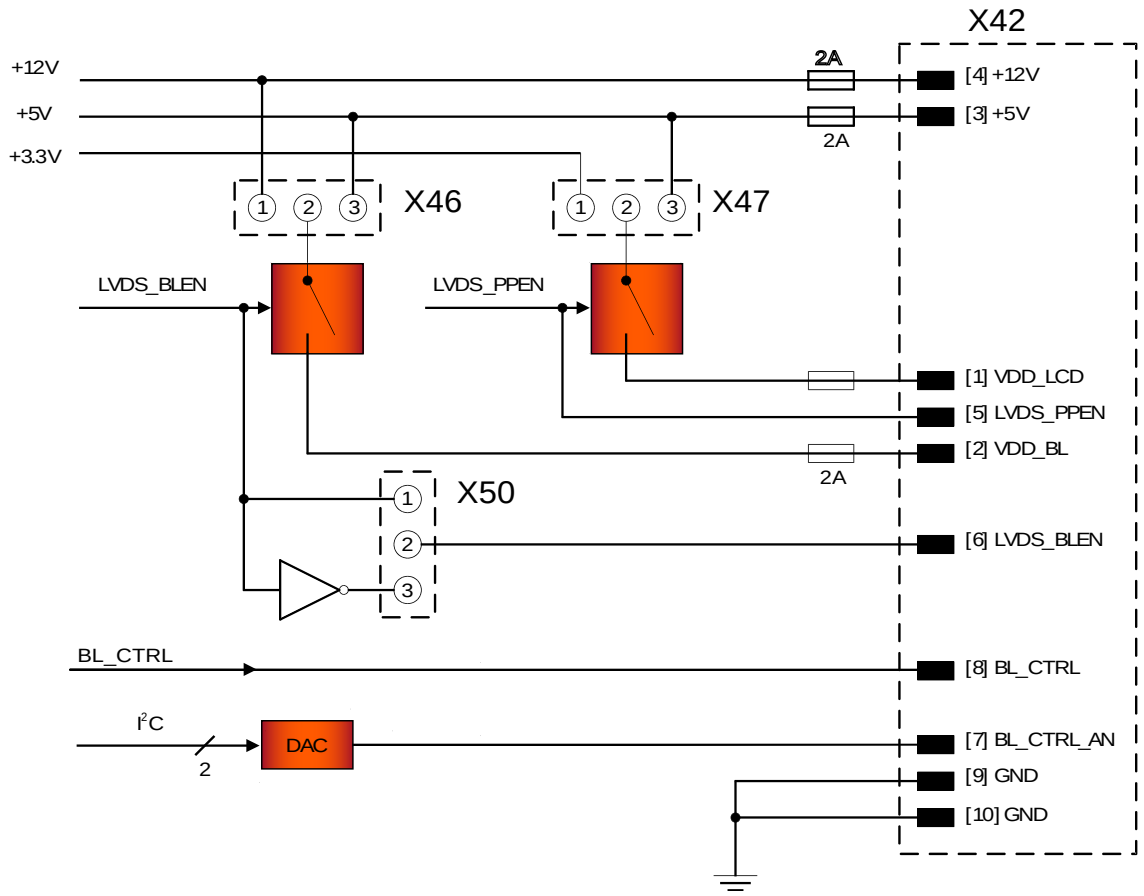


Default Settings:
ALL ON

5.2.11.2 Flat Panel and Backlight Power Supply Connection

The following diagram shows a typical connection possibility for powering panel/backlight by either the VDD_LCD/VDD_BL signals or by using LVDS_PPEN/LVDS_BLEN for external power switches.

- Signals 1-10 correspond to signals 1-10 found on the X42 connector.
- X46, X47 and X50 represent Jumpers X46, X47 and X50 found on the QEVAL 2.0.
- The QEVAL 2.0 carrier board is equipped with a Maxim MAX5362 device referred to in the diagram below as “DAC”.



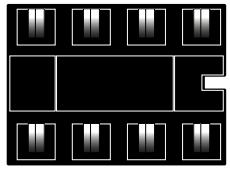
5.2.11.3 Flat Panel Configuration Data

The flat panel configuration data (EPI extended EDID™ 1.3 file) for most common displays is included in the congatec Qseven® CPU module's system BIOS. The customer can also use a customized EPI extended EDID™ 1.3 file that can be stored in a serial EEPROM located on the QEVAL 2.0 (DIL 8 socket U37).

Note

Supported EEPROMs: 24C02, 24C04 and 24C16 at address A0h.

U37
EEPROM Socket

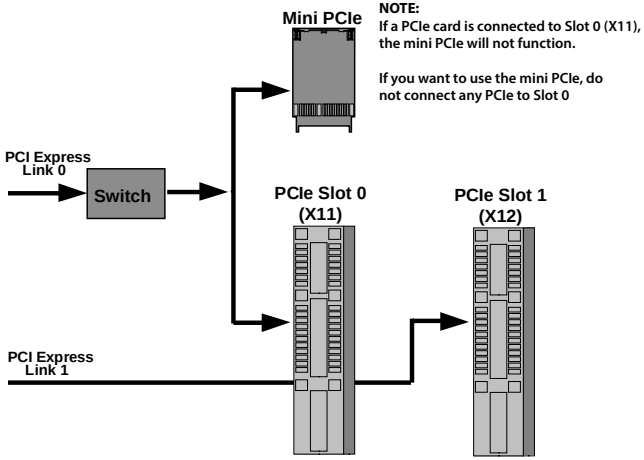


5.2.12 PCI Express Routing

The QEVAL 2.0 supports up to four PCI Express links (PCIe 0-3). PCIe link 0 is shared on the QEVAL 2.0 between PCIe Slot 0 (X11) and mini-PCIe (X31) via a PCIe switch. The table and diagram below describe the routing of the PCI Express links. The table on the next page describes the pinout of each PCI Express slot.

PCI Express Links Routing

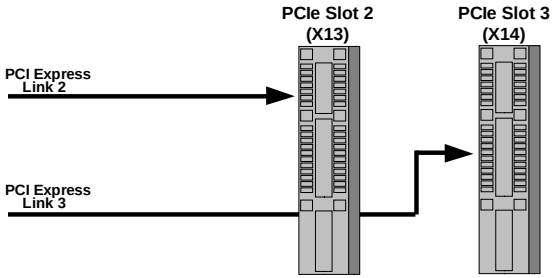
PCIe Link	Originates from	Connected to	Comment
0	Qseven® module	PCIe Slot 0 and miniPCIe via a switch	If you insert a PCIe Card in slot 0, the mini PCIe will not function
1	Qseven® module	PCIe Slot 1 - X12	
2	Qseven® module	PCIe Slot 2 - X13	
3	Qseven® module	PCIe Slot 2 - X14	



Note

The JTAG Interface is not available on any of the PCI Express slot.

If you want to use the mini-PCIe, then do not connect any PCIe card to Slot 0. If a PCIe card is connected to Slot 0 (X11), the mini-PCIe will not function.

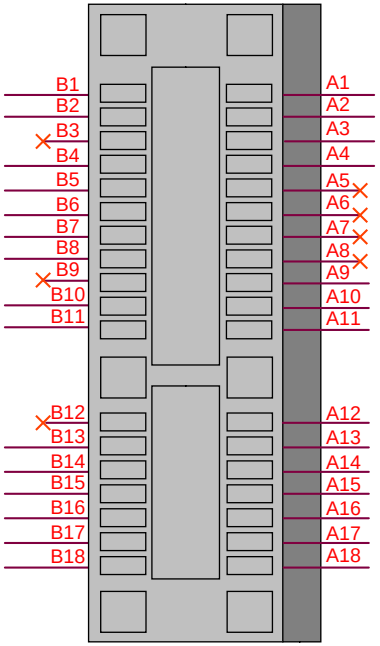


PCI Express Slot 0-3 Pinout Description

PCI Express Slot 0/Link 0 Connector X11				PCI Express Slot 1/Link 1 Connector X12			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT#1_S0	B1	+12V	A1	PRSNT#1_S1
B2	+12V	A2	+12V	B2	+12V	A2	+12V
B3	N.C.	A3	+12V	B3	N.C.	A3	+12V
B4	GND	A4	GND	B4	GND	A4	GND
B5	SMB_CLK	A5	N.C.	B5	SMB_CLK	A5	N.C.
B6	SMB_DAT	A6	N.C.	B6	SMB_DAT	A6	N.C.
B7	GND	A7	N.C.	B7	GND	A7	N.C.
B8	+3.3V	A8	N.C.	B8	+3.3V	A8	N.C.
B9	N.C.	A9	+3.3V	B9	N.C.	A9	+3.3V
B10	+3.3V Standby	A10	+3.3V	B10	+3.3V Standby	A10	+3.3V
B11	WAKE0#	A11	PCIE_RST#	B11	WAKE0#	A11	PCIE_RST#
B12	N.C.	A12	GND	B12	N.C.	A12	GND
B13	GND	A13	PCIE1_CLK+	B13	GND	A13	PCIE2_CLK+
B14	PCIE1_TX+	A14	PCIE1_CLK-	B14	PCIE2_TX+	A14	PCIE2_CLK-
B15	PCIE1_TX-	A15	GND	B15	PCIE2_TX-	A15	GND
B16	GND	A16	PCIE1_RX+	B16	GND	A16	PCIE2_RX+
B17	PRSNT#2_S0	A17	PCIE1_RX-	B17	PRSNT#2_S1	A17	PCIE2_RX-
B18	GND	A18	GND	B18	GND	A18	GND

PCI Express Slot 2/Link 2 Connector X13				PCI Express Slot 3/Link 3 Connector X14			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT#1_S2	B1	+12V	A1	PRSNT#1_S3
B2	+12V	A2	+12V	B2	+12V	A2	+12V
B3	N.C.	A3	+12V	B3	N.C.	A3	+12V
B4	GND	A4	GND	B4	GND	A4	GND
B5	SMB_CLK	A5	N.C.	B5	SMB_CLK	A5	N.C.
B6	SMB_DAT	A6	N.C.	B6	SMB_DAT	A6	N.C.
B7	GND	A7	N.C.	B7	GND	A7	N.C.
B8	+3.3V	A8	N.C.	B8	+3.3V	A8	N.C.
B9	N.C.	A9	+3.3V	B9	N.C.	A9	+3.3V
B10	+3.3V Standby	A10	+3.3V	B10	+3.3V Standby	A10	+3.3V
B11	WAKE0#	A11	PCIE_RST#	B11	WAKE0#	A11	PCIE_RST#
B12	N.C.	A12	GND	B12	N.C.	A12	GND
B13	GND	A13	PCIE3_CLK+	B13	GND	A13	PCIE4_CLK+
B14	PCIE3_TX+	A14	PCIE3_CLK-	B14	PCIE4_TX+	A14	PCIE4_CLK-
B15	PCIE3_TX-	A15	GND	B15	PCIE4_TX-	A15	GND
B16	GND	A16	PCIE3_RX+	B16	GND	A16	PCIE4_RX+
B17	PRSNT#2_S2	A17	PCIE3_RX-	B17	PRSNT#2_S3	A17	PCIE4_RX-
B18	GND	A18	GND	B18	GND	A18	GND

x1 PCI Express Connector



5.2.13 PCI Express Mini Card

The QEVAL 2.0 is equipped with a PCI Express Mini Card socket. PCI Express Mini Card is a unique small size form factor optimized for mobile computing platforms equipped with communication applications such as wireless LAN. The small footprint connector can be implemented on carrier board designs providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradable, standardized PCI Express Mini Card device to the carrier board without additional expenditure of a redesign. The PCI Express Mini Card utilizes USB port 2 and PCI Express link 0. The table below lists the default pinout of the PCI Express Mini Card

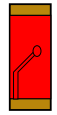
Mini PCI Express Pin Description.

Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3Vaux
3	N.C.	4	GND
5	N.C.	6	+1.5V
7	CLKREQ#	8	N.C.
9	GND	10	N.C.
11	REFCLK-	12	N.C.
13	REFCLK+	14	N.C.
15	GND	16	N.C.
17	N.C.	18	GND
19	N.C.	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	N.C.	46	LED_WPAN#
47	N.C.	48	+1.5V
49	N.C.	50	GND
51	N.C.	52	+3.3Vaux

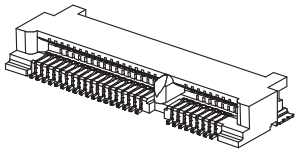
The PCI Mini Card socket has three different red LEDs to indicate the presence of certain area network types. They are as follows:

LED	Indicates
D9	WWAN Wireless Wide Area Network
D10	WLAN Wireless Local Area Network
D11	WPAN Wireless Personal Area Network

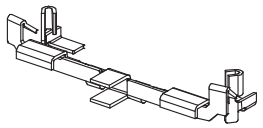
D9-D11



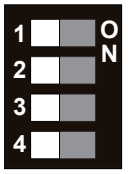
X31



M10



SW9



Default Settings:
ALL OFF

Note

To use a mini PCI Express card that supports USB signals, you must set DIP 3 of Switch SW9 to OFF. To use a mini PCI Express card that

supports PCIe signals, do not connect a PCIe card to PCIe Slot 0

Jumper X32 provides the ability to enable/disable WiFi radio on the PCI Express Mini card.

Jumper X32	Configuration
1 - 2	WiFi Radio is Enabled (default)
2 - 3	WiFi Radio is Disabled

WiFi Radio Enable/Disable (X32)

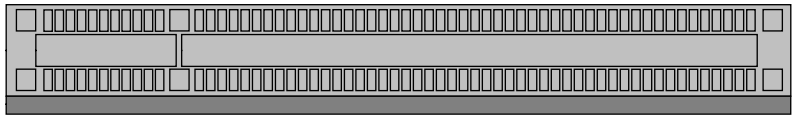
Connector Type

X32: 3 pin 2.54mm grid Jumper.

5.2.14 Digital Display Interface (DDI)

The DDI slot supports DisplayPort, HDMI or DVI cards. The slot supports also congatec's MGCA and HGCA cards.

(X15)



The type of video output depends on the module. If the module supports auto detection then with jumper X22, you can automatically configure the DDI slot for HDMI or DisplayPort.

Jumper X32	Configuration	Description
1 - 2	HDMI_HPD# (default)	Configures DDI for HDMI
2 - 3	DP_HPD#	Configures DDI for DisplayPort

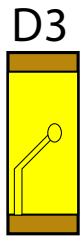
HDMI / DisplayPort (X22)

Note

You can not use ADD2 card or PEG card on the DDI slot.

5.2.15 SDIO Interface

The Qseven® module's SDIO interface is used on the QEVAL 2.0 to provide a SD/MMC card socket. Yellow LED D3 indicates activity on the SDIO interface.

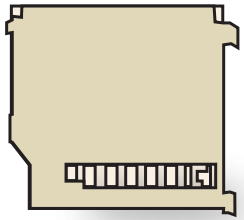


5.2.15.1 SD/MMC Card Socket

The QEVAL 2.0 provides one SD/MMC socket (CN4). The following table lists the pinout of socket CN4.

Pin	Signal	Pin	Signal
1	SDIO_WP	9	+3.3V
2	SDIO_CD	10	GND
3	SDIO Data Line 1	11	SDIO Data Line 5
4	SDIO Data Line 0	12	SDIO_CMD
5	SDIO Data Line 7	13	SDIO Data Line 4
6	GND	14	SDIO Data Line 3
7	SDIO Data Line 6	15	SDIO Data Line 2
8	SDIO CLK		

CN4



5.2.16 CAN Bus

The QEVAL 2.0 provides a Controller Area Network bus interface via a 5 pin header (X10). The CAN bus comes from Qseven® module and is connected to header X10 through CAN transceiver SN65HVD232. Jumper X9 enables or disables CAN bus termination.

Pin	Signal
1	+12V
2	CAN Low
3	GND
4	CAN High
5	N.C.

CAN (X10)

Jumper X9	Configuration
1 - 2	CAN termination Enabled
2 - 3	CAN termination Disabled (default)

CAN Termination (X9)

Connector Type

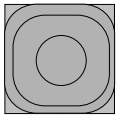
X10: 5 pin 2.54mm grid female, X9: 2.54mm grid Jumper.

6 Additional Features

6.1 Power Button

The Qseven® module performs a power up sequence when you press this button . The power button is connected to the Qseven® module's PWRBTN# signal.

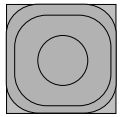
Pwr On (M3)



6.2 Sleep Button

The Qseven® module enters a sleep state when you press this button. The sleep button is connected to the Qseven® module's SLP_BTN# signal.

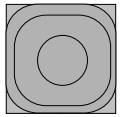
Sleep (M5)



6.3 Reset Button

When you press this button, the Qseven® module and all components connected on the QEVAL 2.0 will perform a hard reset. The reset button is connected to the Qseven® module's RSTBTN# signal.

Reset (M4)

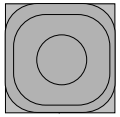


6.4 LID Button

Pressing the LID button creates a low active signal used by the ACPI operating system to detect a LID switch and to bring the system into either a sleep state or to wake it up again. The LID button is connected to the Qseven® module's LID_BTN# signal.

External LID switch can be connected to connector X18.

LID (M6)



Connector Type

X18: 2 pin 2.54mm grid female.

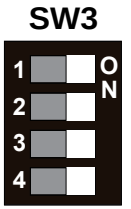
LID (X18)

6.5 Switch SW3

With switch SW3, you can enable or disable the fan speed control (FAN_PWMOUT), panel backlight brightness (LVDS_BL_CTRL), speaker (SPKR) and fan tachometer input (FAN_TACHOIN). The FAN_PWMOUT, LVDS_BL_CTRL and SPKR signals can be used as General Purpose PWM Output and the FAN_TACHOIN signal as General Purpose Timer Input. To do this, you must disable switch SW3.

DIP Switch SW3

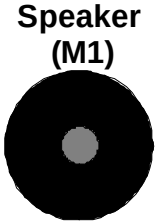
DIP Switch	Status	Description
1	ON OFF	Enable LVDS_BL_CTRL Disable LVDS_BL_CTRL
2	ON OFF	Enable FAN_PWMOUT Disable FAN_PWMOUT
3	ON OFF	Enable SPKR Disable SPKR
4	ON OFF	Enable FAN_TACHOIN Disable FAN_TACHOIN

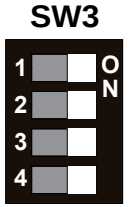


Default Settings:
ALL ON

6.6 PC Speaker

The board-mounted speaker provides audible error code (beep code) information during POST. The speaker is connected to the Qseven® module's SPEAKER signal. To disable the onboard speaker, set DIP 3 of switch SW3 to OFF.



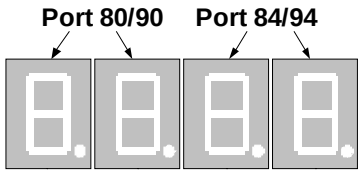


Default Settings:
ALL ON

6.7 Debug Display

During POST (Power On Self Test), the BIOS generates diagnostic progress codes (POST-codes) to different I/O ports (usually port 80h). If the POST fails, execution stops and the last POST code generated is left at the respective port. This code is useful for determining the point where an error occurred.

The QEVAL 2.0 decodes these ports and displays their contents on 4 seven-segment displays (D16 to D19).



A list of the POST codes and associated POST test and initialization routines for the BIOS used on congatec Qseven® modules is available at: http://www.congatec.com.

Jumper X44	Configuration
1 - 2	Port 80h and port 84h output (default)
3 - 4	Port 90h and port 94h output

Debug Display Config (X44)

Connector Type

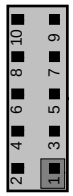
X44: 4 pin 2 row 2.54mm grid Jumper.

6.8 Onboard Module's COM Port

The COM port signals of the Qseven® module are available on the QEVAL 2.0 header connector X30 (COM2). The pin description is shown below:

Pins	Description
1	N.C
2	N.C
3	Receiver
4	Request To Send
5	Transmitter
6	Clear to Send
7	N.C
8	N.C
9	GND
10	N.C

COM2 Header X30



6.9 Internal Use Only Connectors

Connectors X1, X2, X5 and X45 are designated for internal use only and therefore are not available.

Connector Type

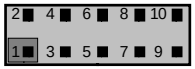
X1, X2: 3 pin 2.54mm grid Jumper.

X5: 10 pin 2 row 2.54mm grid Jumpers.

X45: Not populated.

Internal Use (X1, X2)

Internal Use (X5)



6.10 Ground Probes

The QEVAL 2.0 provides 6 ground probes (M16-M19, M26, M33) that are connected to Ground Potential. These test points make it easier to connect oscilloscope probes and/or multimeter lines to GND when performing measurements on the Qseven® module.

Ground Probe M16-M19, M26, M33

6.11 External System Wake Event

The external system wake event (WAKE#) signal can be found on the feature connector X19. If the Qseven® module does not support the WAKE# signal, then you can bridge connector X3 pins with a jumper to connect the Qseven® module's PCIE_WAKE#.

Pin	Signal
1	WAKE#
2	PCIE_WAKE#

Wake Event (X3)

Connector Type

X3: 2.54mm grid Jumper.

6.12 Fan Connector and Power Configuration

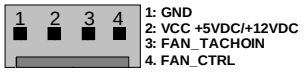
The QEVAL 2.0 provides the ability to connect 5V or 12V cooling fans for the CPU module and system. Connector X20 is for 4pin fan and X21 is for 3pin fan. To enable or disable the fan's control signal (FAN_PMWOUT), use DIP 2 of switch SW3 and to enable or disable the fan's sense control (FAN_TACHOIN), use DIP 4 of switch SW3.

The following tables describe the pinouts and Jumper configuration possibilities.

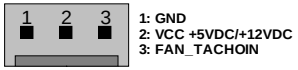
X20 FAN Pin	Signal
1	GND
2	VCC +5VDC/+12VDC
3	FAN_TACHOIN
4	FAN_CTRL

X21 FAN Pin	Signal
1	GND
2	VCC +5VDC/+12VDC
3	FAN_TACHOIN

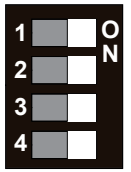
CPU Fan (X20)



SYS Fan (X21)



SW3



Default Settings:
ALL ON

Connector Type

X20: 4 pin 2.54mm grid female fan connector, X21: 3 pin 2.54mm grid female fan connector.

Jumper X48	Configuration
1 - 2	4pin FAN +12VDC (default)
2 - 3	4pin FAN +5VDC

Jumper X51	Configuration
1 - 2	3pin FAN +12VDC (default)
2 - 3	3pin FAN +5VDC

Jumper X52	Configuration
1 - 2	3pin FAN w/o control (default)
2 - 3	3pin FAN with control

X48
X51
X52

Connector Type

X48, X51 and X52: 2.54mm grid Jumper.

Note

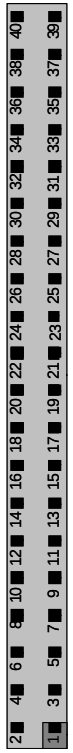
The FAN_TACHOIN signal that originates from the Qseven® module and is connected to pin 3 on connector X20 and X21 of the QEVAL 2.0 must receive two pulses per revolution in order to produce an accurate reading. Therefore, a two pulse per revolution fan is recommended. If both FANs are to be used at the same time, then one FAN must not be connected to FAN_TACHOIN (module has only one TACHOIN input).

VCC on X21 is controlled by the fan's PWM control signal, which originates from the Qseven® module. With Jumper X52, you can disable this control.

6.13 Feature Connector

Pin	Signal	Description	Pin	Signal	Description
1	+5V (750 mA fuse)		2	5V_SB (750 mA fuse)	
3	HDD LED		4	Hard Disk Activity	Shows activity on hard disk interface
5	GP0_I2C_DAT0	General purpose I²C port data I/O line.	6	I2C_CLK1/SMB_CLK	I2C or System Management Bus bidirectional clock line.
7	GP0_I2C_CLK0	General purpose I²C port clock output.	8	I2C_DAT1/SMB_DAT	I2C or System Management Bus bidirectional data line.
9	N.C.		10	GP_PWM_OUT0	General Purpose PWM Output
11	N.C.		12	GP_PWM_OUT1	General Purpose PWM Output
13	PS_ON#	Power Supply On (active low).	14	GP_PWM_OUT2	General Purpose PWM Output
15	SUS_S3#	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	16	GP_1-Wire Bus	General Purpose 1-Wire Bus interface
17	GND	Power Ground	18	GND	Power Ground
19	THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown.	20	SMB_ALERT#	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.
21	N.C.		22	N.C.	
23	SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	24	GP_TIMER_IN	General Purpose Timer Input
25	N.C.		26	SUS_S5#	S5 State: This signal indicates S4 or S5 (Soft Off) state.
27	WDTRIG#	Watchdog trigger signal.	28	THRM#	Input from off-module temp sensor indicating an over-temp situation.
29	WDOUT	Watchdog event indicator	30	N.C.	
31	BATLOW#	Indicates that external battery is low.	32	WAKE#	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.
33	GP2_I2C_DAT2	General purpose I²C port data I/O line.	34	N.C.	
35	GP2_I2C_CLK2	General purpose I²C port clock output.	36	RSTBTN#	Reset Button Input. Active low input. This input may be driven active low by an external circuitry to reset the Qseven® module.
37	GND	Power Ground	38	GND	Power Ground
39	PWBTN#	Power Button: Low active power button input. This signal is triggered on the falling edge.	40	PWGIN	High active input for the Qseven® module indicates that power from the power supply is ready.

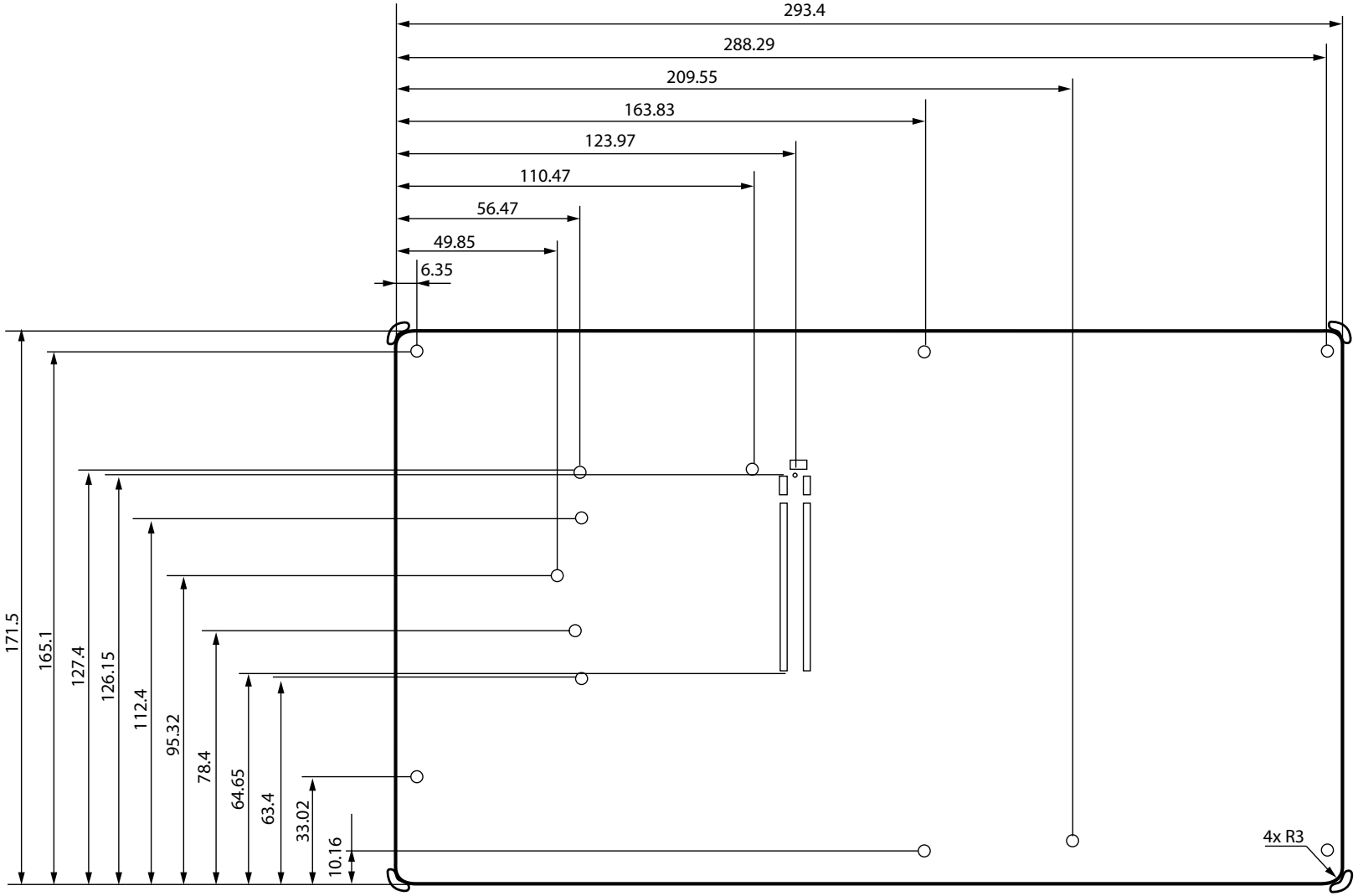
Feature (X19)



Connector Type

X19: 40 pin, 2 row 2.54mm grid female.

7 QEVAL 2.0 Mechanical Drawing



All dimensions are in mm

8 Industry Specifications

The list below provides links to industry specifications that should be used as reference material when designing a Qseven® carrier board.

Specification	Link
Qseven® Specification	http://www.qseven-standard.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
MMC Multimedia Card Association	http://www.mmca.org
SD Card Association	http://www.sdcard.org
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
High Definition Audio Specification, Rev. 1.0	http://www.intel.com/standards/hdaudio/
LVDS Owner's Manual	http://www.national.com
Extended Display Identification Data Standard Version 1.3 (EDID™)	http://www.vesa.org
Enhanced Display Data Channel Specification Version 1.1 (DDC)	http://www.vesa.org
IEEE standard 802.3ab 1000BASE T Ethernet	http://www.ieee.org/portal/site
Advanced Configuration and Power Interface Specification Rev. 3.0a	http://www.acpi.info/